MERG DCC accessory decoder – Firmware version 5 (ACC5)

The firmware version (ACC4) runs either the Pulse decoder (with inbuilt CDU) or the 'steady state' decoder with DC outputs. It is compatible with both the MERG accessory encoder and commercial systems like Lenz. However, both of these assume that the decoder will be used to drive point motors with the outputs operating in pairs. Hence it is not possible to activate the 8 outputs individually as either one side or the other of a 'pair' is always active. Also, Lenz systems do not send 'deactivate' commands so an output cannot be turned off and it is assumed that activating one output of a pair will automatically turn off the other side. This must be a property of the decoder and ACC4 had the 'toggle' mode introduced for this purpose. (The MERG encoder does send 'deactivate' commands).

From its early stages, the MERG accessory decoders had the capability to operate all 8 outputs independently but this could not be achieved with command stations assuming 'paired' operation.

ACC5 now has an option which allows a single decoder board to act as two separate decoders. In this 'dual' mode, outputs 1 to 4 are controlled by one decoder address and outputs 5 to 8 are controlled by a different address. This enables a single decoder board to have all 8 outputs individually controlled by systems that assume paired operation. Activating side 'b' of an output will turn that output on. Activating side 'a' of that output will turn it off so each decoder 'address' works 4 outputs.

For ACC5, an activate to point 1 (001) will turn output 1 on and an activate to point 0 (000) will turn output 1 off. When used with the MERG encoder, this means the output is on when the matrix switch is open and off when the switch is closed. This arrangement was to maintain Lenz compatibility where a '+' will turn output 1 on and a '-' will turn it off. With the MERG encoder, 8 individual on/off switches will control the 8 outputs of a single decoder board.

The main purpose of this arrangement is for light or signal operation. The 'steady state' MERG decoder board has outputs suited for 12v bulbs or LEDs (resistors on the decoder board). However, the same board could drive 8 points using the Servo4 drivers as these only need an on / off input.

Method of operation

ACC5 can work in either single or dual mode dependent on the setting of bit 7 (the MSB) of CV545 (CV33). As this cannot be set using 'register' mode programming, it requires a programmer capable of accessing CV545 or CV33. Either page mode or direct mode are accepted.

To use as ACC4 (single mode) set CV545, bit 7 off. CV545 also contains the 'toggle' bits for Lenz system operation. To use in dual mode, set bit 7 of CV545. In this mode, the toggle bits are ignored.

To set the addresses.

Set CV545 bit 7 off. Then program the decoder as usual with address data at CV513 and CV521. CV513 (CV1) contains the low 6 bits of the address. (0 to 63) and CV521 (CV9) contains the high three bits (0 to 7). When in dual mode, this address controls outputs 1 to 4. CV514 (CV2) should be left at 255 so all outputs are active and CVs 515 to 518 set the on time of the outputs. Note, with the present code, CV515 sets the time for outputs 1 and 2, CV516 for 3 and 4 etc. irrespective of mode. This may be modified in future so all 8 outputs

can have different times. When operating lights or signals it will be normal to set the timing CVs to 0 so the output is continuous.

Now set CV545 bit 7 to 1. Repeat the address programming for the decoder that will control outputs 5 to 8. Obviously this second address should be different from the first but it doesn't have to be consecutive and can be higher or lower than the first address.

The decoder is now set up for dual mode. Reading the CVs in this mode will return the values for the second address. You will need to clear CV545 bit 7 to 0 in order to read the CVs for the first address. Clearing this bit also places the decoder in the conventional 'single' mode which would be used for points or other applications requiring paired outputs.

The following alternative CV's and register addresses are supported.

NMRA CV	Alt CV	Register
CV513	CV1	R1 (Address low 6 bits))
CV514	CV2	(not available in register mode)
CV515	CV3	R2 (F1 on time)
CV516	CV4	R3 (F2 on time)
CV517	CV5	R4 (F3 on time)
CV518	CV6	R5 (F4 on time)
		R6 (Page register)
CV519	CV7	R7 (version)
CV520	CV8	R8 (manufacturer)
CV521	CV9	Address high 3 bits (not available in register mode)
CV541	CV29	Configuration (not available in register mode)
CV545	CV33	Sets toggle function for Lenz compatibility and dual mode option. Not available in register mode

No other CVs are supported.

CV545 (CV33)	bit 0	sets toggle mode for OP1/2
	bit 1	sets toggle mode for OP3/4
	bit 2	sets toggle mode for OP5/6
	bit 3	sets toggle mode for OP7/8
	bit 7	sets dual decoder mode

Note: The toggle is for Lenz compatibility in single decoder mode only. These bits are ignored in dual mode. For compatibility with the MERG encoder, they should be set to 0.

The ACC5 code on the MERG website has the default CVs set for dual mode at decoder addresses 1 and 2.