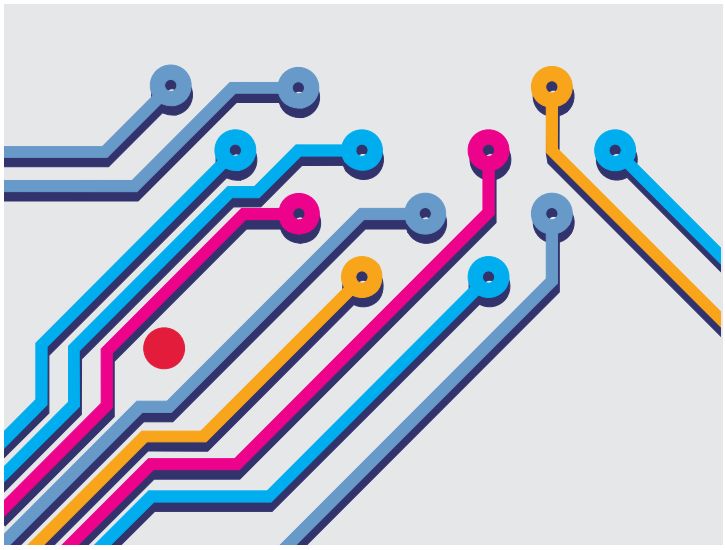
# Advanced PCB™

## *Printed Circuit Board Design System for Windows*



***Professional 32-bit PCB design system for Windows***

***Options:*** ***Advanced PCB, with design automation & productivity tools***
***Advanced Place, intelligent component auto placement***
***Advanced Route, 16 layer rip-up / retry autorouting***

Protel Technology

***On-line Appendices***

**Advanced PCB**



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## PCB file format specification

Advanced PCB provides three options when saving files. The default binary format generates a compact database, which loads and saves file data efficiently. Files are also saved using two text formats: Protel Text and Autotrax.

The Protel Text option generates the PCB FILE 6 v. 2.40 database – a straightforward ASCII text-only format that supports translation and other direct manipulation of PCB file data. For example, users can modify ASCII files with a text editor, as long as a few simple rules are followed. Firstly, the exact syntax of the format must be preserved.

This section describes the format completely. If you have a problem with a user-edited file, it is probably due to some violation of the format, either a syntax error or out-of-range data. Unless you edit carefully, it can be difficult to diagnose and correct mistakes. However, Advanced PCB does perform a file validation check each time an ASCII source PCB file is opened. Validation checks for out-of-range coordinates. The legal range is generally 0–99999.999 mils, less the dimensions of any primitive or component. Validation also checks internal netlist and connection data. Advanced PCB will attempt to correct any problems, to make the file loadable, for example, out of range coordinates and layer numbers are re-assigned within the legal range.

If connectivity problems are encountered during file loading, a warning message will be displayed and the internal netlist will be stripped from the PCB file and be written into a separate (filename).NET file. In this file, the string **ERROR** will be used to identify bad nodes. Problems are listed in a separate report file (filename).VLD.

Also, the text file must be maintained in pure ASCII format.

- Do not save edited files with the "hidden" characters and other format data that is routinely added to word processor files. Saving the post-edited file using a "Text Only" format option usually prevents this problem.

There are six sections in the file: header, components, primitives, netlist data, file defaults and an end of file marker. Contents of a sample file are described below.

- External coordinate and dimension values, unless otherwise indicated, are expressed in 0.001 mil units (1 unit = 0.000001 inch). All values are stored in this format. Metric values are converted from imperial units.

See the section, Definitions, for additional descriptions of individual primitive attributes. Syntax of component primitives and free primitives is identical: component primitives are marked CS (component string), CP (component pad) etc. Free primitives are headed FS (free string), FT (free track), etc.

These examples of PCB file data conforms to the order of data that will be found in a representative file, but is limited to a single item of each data type. The beginning of an ASCII file looks like:

### The file header

```
PCB FILE 6 VERSION 2.40

282 1871 370 88 14 56 36 0 428 0
```

The PCB file header indicates the start of the file.

This line includes these PCB file attributes:

| | |
|---|---|
| 282 | Connection count (number of connections in file). |
| 1871 | Track count. |
| 370 | Node count. |
| 88 | Net count. |
| 14 | Arc count. |

| | |
|---|---|
| 56 | Via count. |
| 36 | Component count. |
| 0 | Fill count. |
| 428 | Pad count. |
| 0 | String count. |

### The component section

| | |
|---|---|
| COMP | Marks the beginning of data for each component. |
| DIP40 | Pattern (name of footprint in component library) of first component in the file. Pattern name must be between 1-12 characters in length. No spaces are allowed. This line is followed by: |

***0 1 2580000 1180000 1 0 2525000 1155000 4535000 1805000***

| | |
|---|---|
| | This line obove includes these component attributes: |
| 0 | Selection status (0 = unselected, 1 = selected). |
| 0 | DRC highlight status (0 = off, 1 = on). |
| 2525000 1180000 | Reference point x, y coordinates (range: 0-99999999). |
| 1 | Designator display status (0 = hide, 1 = display). |
| 1 | Comment display status (0 = hide, 1 = display). |
| 0 | Placement status (0 = free to move, 1 = fixed in place). |
| 2525000 1155000 4535000 1805000 | Minimum x, min y, maximum x, max y coordinates (dimensions of component, excluding the designator and comment). |
| CS | Marks component string primitive. This component designator must be present for each component. |

***0 0 2500000 1180000 60000 90.000 0 1 17 2434019 1174000 2506000 1285967***

| | |
|---|---|
| | This line includes these designator string attributes: |
| 0 | Selection status (0 = unselected, 1 = selected). |
| 0 | DRC highlight status (0 = off, 1 = on). |
| 2500000 1180000 | Reference point x, y coordinates (range: 0-99999999 ). |
| 60000 | Height of string (range: 10-999999). |
| 90.000 | Rotation of string (0.001-360.000 degrees). |

| | |
|---|---|
| 0 | Orientation of string (0 = normal, 1 = flip in x axis). |
| 1 | Font (1 = default, 2 = Sans Serif, 3 = Serif). |
| 17 | Layer (range: 1-34, see Definitions, below). |
| 2434019 1174000 2506000 1285967 | Minimum x, min y, maximum x, max y coordinates of string. |
| U5 | Content of the (above defined) string, Designator must be between 1-8 characters. No spaces are allowed in designator strings. |
| CS | Marks beginning of the second component string data. The second component string (if present in the data) always represents the component comment field and is optional. |

***0 0 2720000 1560000 60000 360.000 0 1 17 2714000 1554000 3185851 1625980***

This line includes the comment string attributes. They are identical to the attributes of the first (designator) string.

| | |
|---|---|
| Z80A CPU | Contents of the comment string (range: 0-32 characters, including spaces). |
| CP | Marks component pad primitive. |

***0 0 2580000 1780000 50000 50000 1 32000 0 34 68 0 0***

***This line incudes these pad attributes fields:***

| | |
|---|---|
| 0 | Selection status (0 = unselected, 1 = selected). |
| 0 | DRC highlight status (0 = off, 1 = on). |
| 2580000 1780000 | Pad center x, y coordinates (range: 0-99999999). |
| 50000 50000 | Pad x, y size (range: 2-500000). |
| 1 | Pad shape (0 = rounded, 1 = rectangular, 2 = octagonal, 6 = terminator). |
| 32000 | Pad hole diameter (range: 0-500000). |
| 0 | Power plane status of pin. 0 = no connection to plane, see Definitions. |
| 34 | Pad layer (range: 1-34) 34 = Multi-layer, see Definitions. |
| 68 | Net number assigned to pin, see Definitions. |

| | | |
|---|---|---|
| | 0 | Connection terminator, see Definitions. |
| 40 | | Pad designator (component pin number). Can be up to 4 alphanumeric characters in length. This field can also be empty or null (0). |
| CT | | Marks component track primitive. |

***0 0 5850000 4270000 5950000 4270000 12000 17 1 0 0***

***Component track attribute fields include:***

| | | |
|---|---|---|
| | 0 | Selection status (0 = unselected, 1 = selected). |
| | 0 | DRC highlight status (0 = off, 1 = on). |
| | 5850000 4270000 | Track start point x, y coordinates (range: 0-99999999). |
| | 5950000 4270000 | Track end point x, y coordinates (range: 0-99999999). |
| | 12000 | Track width (range: 1-99999999). |
| | 17 | Track layer (range: 1-34), see Definitions. |
| | 1 | Track route status ( 0 = autorouted, 1 = user routed). |
| | 0 | Net number assigned to track, see Definitions. |
| | 0 | Connection number, see Definitions. |
| | 0 | Polygon number, see Definitions |
| CT | | Marks next component track primitive. |

***0 0 5850000 4170000 5950000 4170000 12000 17 1 0 0 0 0***

| | |
|---|---|
| | Data for next component track, as above. |
| ENDCOMP | Marks end of the data for each component. |

### Free primitives section

Advanced PCB uses six types of primitives: arcs, fills, pads, strings, tracks and vias. These are the basic building blocks for all design work. These primitives can be used as individual entities (free primitives) or grouped together to form components (component primitives, as described in the previous section). A special seventh "primitive" is the polygon, used to define copper pour areas. Although polygons are composed of arcs, tracks and fills, they have editable fields, similar to components, described below.

| | |
|---|---|
| FA | Marks free arc primitive. |
| 0 0 2400000 5080000 40 90.000 180.000 10 16 1 0 0 | |
| | Free arc attributes. Each field is described below: |
| 0 | Selection status (0 = unselected, 1 = selected). |
| 0 | DRC highlight status (0 = off, 1 = on). |
| 2400000 5080000 | Arc center x, y coordinates (range: 0-99999999). |
| 40 | Arc radius (range: 1-99999999). |
| 90.000 | Arc start angle (range: 0.001-360.000 degrees). |
| 180.000 | Arc end angle (range: 0.001-360.000 degrees). |
| 10 | Arc line width (range: 1-999999). |
| 16 | Arc layer (range: 1-34), see Definitions. |
| 1 | Net number, see Definitions. |
| 0 | Connection number, see Definitions. |
| 0 | Polygon number, see Definitions. |
| FF | Marks free fill primitive. This is also known as an area fill - rectangular (solid copper) fill that can be placed on any layer. |
| 0 0 1980000 2410000 2240000 2760000 14 0 0 | Free fill attributes. Each field is described below: |
| 0 | Selection status (0 = unselected, 1 = selected). |
| 0 | DRC highlight status (0 = off, 1 = on). |
| 1980000 2410000 | Fill first corner x, y coordinates (range: 0-99999999). |
| 2240 2760 | Fill opposite corner x, y coordinates. |
| 14 | Fill layer (range: 1-34), see Definitions. |

| | |
|---|---|
| 0 | Net number, see Definitions. |
| 0 | Polygon number, see Definitions. |

***FP*** ***Marks free pad primitive - pads that can be placed independently from components, on any layer.***

***1 0 2780000 2480000 50000 50000 1 50000 50000 1 50000 50000 1 32000 0 34 24 0***

***Pad attributes. This line includes the following attributes:***

| | |
|---|---|
| 1 | Selection status (0 = unselected, 1 = selected). |
| 0 | DRC highlight status (0 = off, 1 = on). |
| 2780000 2480000 | Pad center x, y coordinates (range: 0-99999999).* |
| 50000 50000 | Pad x, y size (range: 2-500000).* |
| 1 | Pad shape (0 = rounded, 1 = rectangular, 2 = octagonal, 6 = terminator, see Definitions).* |
| | *Three sets of size/hole/shape values are included. The first set is for Top layer, second set is Mid-layer 1-14, 3rd is for Bottom layer. |
| 32000 | Pad hole diameter (range: 0-500000). |
| 0 | Power plane status of pin (0 = no connection to plane), see Definitions. |
| 34 | Pad layer (range: 1-34), see Definitions. |
| 24 | Net number assigned to pin, see Definitions. |
| 0 | Connection terminator, see Definitions. |

FS Marks free string primitive.

0 0 4362000 4340000 60000 90.000 0 1 17 4296019 4334000 4368000 4445967

This line includes the free string attributes:

| | |
|---|---|
| 0 | Selection status (0 = unselected, 1 = selected). |
| 0 | DRC highlight status (0 = off, 1 = on). |
| 4362000 4340000 | Reference point x, y coordinates (range: 0-99999999). |
| 60000 | Height of string (range: 10-999999). |
| 90.000 | Rotation of string (range: 0.001-360.000 degrees). |

| | |
|---|---|
| 0 | Orientation of string (0 = normal, 1 = flip in x axis). |
| 1 | Font (1 = default, 2 = Sans Serif, 3 = Serif). |
| 17 | Layer (1-34 range, see Definitions, below). |
| 4296019 4334000 4368000 4445967 | Minimum x, min y, maximum x, max y string coordinates. |
| Sample of free string | This is the contents of the string, up to 32 characters, including spaces. |
| FT | Marks free track primitive. |

***0 0 2340000 1540000 2340000 2040000 10000 13 0 48 30 0***

***Free track attributes. Each field is described below:***

| | |
|---|---|
| 0 | Selection status (0 = unselected, 1 = selected). |
| 0 | DRC highlight status (0 = off, 1 = on). |
| 2340000 1540000 | Track start point x, y coordinates (range: 0-99999999). |
| 2340000 2040000 | Track end point x, y coordinates (range: 0-99999999). |
| 10000 | Track width (range: 1-999999). |
| 13 | Track layer (range: 1-34), see Definitions. |
| 0 | Track route status ( 0 = autorouted, 1 = user routed). |
| 48 | Net number assigned to track, see Definitions. |
| 30 | Connection number, see Definitions. |
| 0 | Polygon number, see Definitions |
| FV | Marks free via primitive. These are vias that can be placed on the Multi-layer or on any layer pair. |

***1 0 4720000 1760000 50000 28000 1 0 2 11***

***Via attributes. Each field is described below:***

| | |
|---|---|
| 1 | Selection status (0 = unselected, 1 = selected). |
| 0 | DRC highlight status (0 = off, 1 = on). |
| 4720000 1760000 | Via center x, y coordinates (range: 0-99999999). |
| 50000 | Via diameter (range: 2-5000000). |
| 28000 | Via hole diameter (range: 0-500000). |
| 1 | Via route status ( 0 = autorouted, 1 = user routed). |

| | | |
|---|---|---|
| | 0 | Layer pair (0 = Multi-layer), see Definitions. |
| | 2 | Net number assigned to via, see Definitions. |
| | 11 | Connection number, see Definitions. |
| *PG* | | *Marks special polygon object which can include arcs, fills and tracks.* |
| *1* | | *Polygon layer number (range: 1-34).* |
| *0* | | *Net number assigned to Polygon, see Definitions.* |
| *0 1 1 0* | | *This line includes these attributes:* |
| | *0* | *Remove dead copper (0 = false, 1 = true).* |
| | *1* | *Horizontal tracks (0 = false, 1 = true).* |
| | *1* | *Vertical tracks (0 = false, 1 = true).* |
| | *0* | *Arcs/octagons at pads (0=arcs, 1=ocatagons).* |
| *0* | | *Fills for tracks (0 = false, 1 = true)* |
| *20000* | | *Polygon grid size (range: 1-99999).* |
| *10000* | | *Polygon track/arc width (range: 1-99999).* |
| *9* | | *Number of vertices in polygon.* |
| *15260000 40380000* | | *Coordinates of first vertex (range: 1-99999999).* |
| *15260000 53000000* | | *Coordinates of second vertex (range: 1-99999999).* |
| *(coordinates listed for each vertex)* | | |
| *1 0 0 1 1 0 0 0 0 0* | | *Track or arc used for each perimeter segment (0 = track, 1 = arc).* |

***FA*** ***Marks the first arc in the polygon.***

```
0 0 27140000 49620000 3240000 270.000 360.000 10000 1 0 0 1
```

***Arc data (see Free Arcs, above).***

***FT*** ***Marks the first track in the polygon.***

```
0 0 15280000 40540000 15280000 53000000 10000 1 0 0 0
```

***Track data (see Free Tracks, above).***

### Netlist section

Advanced PCB stores connectivity information in the form of an internal netlist, attached to the end of the PCB file. This internal list is similar to, but should not be confused with the external netlist format generated by a schematic capture program. Note that connection and node information is stored in an efficient shorthand, rather than using the full component designator, etc.

| | | |
|---|---|---|
| NETDEF | | Marks the beginning of a net. |
| RESET | | Name of net. |
| 0 0 2 2 | | This line sets net routing defaults, including: |
| | 0 | Track width used to route this net (range: 0-999999).* |
| | 0 | Via diameter used to route this net (range: 0-999999).* |
| | 2 | Net reconnect method (optimization), see Definitions. |
| | 2 | Route priority, 0 is highest priority, (range: 0-4). |
| ( | | Parentheses (open) delimits first node in net. |
| 1 3 | | First component/pin node in net. This line includes these attributes: |
| | 1 | Component number. This number is automatically assigned, based on the order of the database. |
| | 3 | Component pad (or pin) number. |
| 3 2 | | Second component/pin in net. |
| 2 2 | | Third component/pin in net. |
| 4 2 | | Fourth component/pin in net (etc). |
| ) | | Parentheses (close) delimits end of net. |
| | | |
| { | | Braces (open) delimits beginning of optimized node information. |
| 3 4 8 0 0 | | Data for the first connection in net: |
| | 3 4 | Marks connection for nodes 3 and 4, as shown above. |
| | 8 | Connection flag (4-bit number), see Definitions. |
| | 0 | Un-used field. Zero (0) is place holder. |

| | |
|---|---|
| | 0 Routed by code (identifies router pass), see Definitions. |
| 1 3 8 0 0 | Data for next connection, as described above (etc.). |
| } | Braces (close) delimits end of connection information. |
| 1 2 0 | This line includes the following fields: |
| | 1 Source node (indicates first pin in net). |
| | 2 Terminator node (indicates last pin in net). |
| | 2 Class of net. see Definitions. |
| 34 | Net layer assignment (34 = Multi-layer; 23 = Power plane 1; 24 = Power plane 2; 25 = Power plane 3; 26 = Power plane 4). |

### Defaults section

The last section of the Advanced PCB file format stores a number of settings and user defaults that were active when the file was saved. This information allows information relevant to the design file, for example the active layers and grid settings, to be restored when the file is re-loaded. A separate, larger set of system defaults are stored in the PFW.INI file. These items include output and other system-level options.

| | | |
|---|---|---|
| DEFAULTS | | Marks the beginning of the defaults section. |
| 0 0 | | Origin of file x, y (range: 0-99999999). |
| 2500 4440 | | Cursor position x,y (range: 0-99999999). |
| 1 | | Scroll bars (0 = hide, 1 = show). |
| 1 1 1 | | Snap grid defaults include the following parameters: |
| | 1 | Snap grid units (0 = metric, 1 = mils). |
| | 1 | Visible grid 2 units (0 = metric, 1 = mils). |
| | 1 | Visible grid 1 units (0 = metric, 1 = mils). |
| 1000 20 20 20 | | Grid defaults data, including: |
| | 1000 | Visible grid pitch (range: 1-99999.999 mils). |
| | 20 | Visible grid 1 pitch (range: 1-99999.999 mils). |
| | 20 | Autoplace Move to Grid pitch (range: 1-999.999 mils). |
| | 20 | Snap grid pitch (range: 1-999.999). |
| 1 20 | 1 | Current layer and zoom level parameters: |
| | 20 | Current layer (range: 1-34) |
| | | Zoom level (range: 0.1-400 units) |
| 1 | | Top layer (0 = off, 1 = on) |
| 0 | | Mid-layer 1 (0 = off, 1 = on) |
| 0 | | Mid-layer 2 (0 = off, 1 = on) |
| 0 | | Mid-layer 3 (0 = off, 1 = on) |
| 0 | | Mid-layer 4 (0 = off, 1 = on) |
| 0 | | Mid-layer 5 (0 = off, 1 = on) |
| 0 | | Mid-layer 6 (0 = off, 1 = on) |

| | |
|---|---|
| 0 | Mid-layer 7 (0 = off, 1 = on) |
| 0 | Mid-layer 8 (0 = off, 1 = on) |
| 0 | Mid-layer 9 (0 = off, 1 = on) |
| 0 | Mid-layer 10 (0 = off, 1 = on) |
| 0 | Mid-layer 11 (0 = off, 1 = on) |
| 0 | Mid-layer 12 (0 = off, 1 = on) |
| 0 | Mid-layer 13 (0 = off, 1 = on) |
| 0 | Mid-layer 14 (0 = off, 1 = on) |
| 1 | Bottom layer (0 = off, 1 = on) |
| 1 | Top overlay (0 = off, 1 = on) |
| 0 | Bottom overlay (0 = off, 1 = on) |
| 0 | Top paste (0 = off, 1 = on) |
| 0 | Bottom paste (0 = off, 1 = on) |
| 0 | Top solder (0 = off, 1 = on) |
| 0 | Bottom solder (0 = off, 1 = on) |
| 0 | Power Plane 1 (0 = off, 1 = on) |
| 0 | Power Plane 2 (0 = off, 1 = on) |
| 0 | Power Plane 3 (0 = off, 1 = on) |
| 0 | Power Plane 4 (0 = off, 1 = on) |
| 0 | Drill guide layer (0 = off, 1 = on) |
| 1 | Keep out layer (0 = off, 1 = on) |
| 0 | Mechanical layer 1 (0 = off, 1 = on) |
| 0 | Mechanical layer 2 (0 = off, 1 = on) |
| 0 | Mechanical layer 3 (0 = off, 1 = on) |
| 0 | Mechanical layer 4 (0 = off, 1 = on) |
| 0 | Drill drawing layer (0 = off, 1 = on) |
| 1 | Multi-layer 1 (0 = off, 1 = on) |
| 0 | (field not used) |
| 1 | Rats nest layer (0 = off, 1 = on) |

| | | |
|---|---|---|
| 1 | DRC errors layer 1 | (0 = off, 1 = on) |
| 1 | not used | |
| 1 | Visible grid 1 | (0 = off, 1 = on) |
| 1 | Visible grid 2 | (0 = off, 1 = on) |
| 1 | Pad holes display | (0 = off, 1 = on) |
| 1 | Via holes display | (0 = off, 1 = on) |
| ENDPCB | End of file marker. | |

### Definitions

The definitions in this section explain some of the functions of data in the file format Ranges of legal values, where applicable, are shown in parentheses at the end of the definition.

***Class (net)*** Nets can be grouped by Class (whole number: 0–32,768). Advanced SB Route allows assignment of design rules to a group of nets assigned to a Class.

***Connection flag*** This is a 4 bit number that appears in the connection data in the attached netlist. These values are available for this number:

Bit 0 0 = Unrouted 1 = Routed

Bit 1 1 = Failed last pass

Bit 2 1 = Ripped Up

Bit 3 1 = Shown 0 = Hidden

***Connection number*** Internally assigned reference number stored in the attached netlist (see Netlist section for example). Refers to the nth connection in a net (1 = 1st connection, 2 = 2nd, etc.).

***Connection terminator*** Designates a special pad used to maintain the ratsnest for a partially routed connection.

***DRC highlight status*** DRC Layer highlight status is toggled by the Design Rule Checking unit. Primitives that have clearance violations are highlighted (displayed) on the DRC layer (0 = off, 1 = on).

***End angle (arcs)*** Defines the ending angle of an arc (in degrees) where the 3 o'clock position from the arc center is 0 degrees. The angle is measured in a counter-clockwise rotation, so that an end angle at the 12 o'clock position would be 90 (0.001-360.000) .

***Layer*** Defines the layer occupied by a primitive (range: 1-34), values are:

| | |
|---|---|
| 1 = Top layer | 18 = Bottom Silkscreen |
| 2 = Mid layer 1 | 19 = Top Paste Mask |
| 3 = Mid layer 2 | 20 = Bottom Past Mask |
| 4 = Mid layer 3 | 21 = Top Solder Mask |
| 5 = Mid layer 4 | 22 = Bottom Solder Mask |
| 6 = Mid layer 5 | 23 = Plane 1 |
| 7 = Mid layer 6 | 24 = Plane 2 |
| 8 = Mid layer 7 | 25 = Plane 3 |
| 9 = Mid layer 8 | 26 = Plane 4 |
| 10 = Mid layer 9 | 27 = Drill Guide |
| 11 = Mid layer 10 | 28 = Keep Out layer |
| 12 = Mid layer 11 | 29 = Mechanical layer 1 |
| 13 = Mid layer 12 | 30 = Mechanical layer 2 |
| 14 = Mid layer 13 | 31 = Mechanical layer 3 |
| 15 = Mid layer 14 | 32 = Mechanical layer 4 |
| 16 = Bottom layer | 33 = Drill Drawing |
| 17 = Top Silkscreen | 34 = Multi layer |

***Layer pair*** Defines the via type as Through Hole or Blind/Buried (0-8).

0 = Multilayer (all layers)

1 = Top - Mid 1 pair

2 = Mid 2 - Mid 3 pair

3 = Mid 4 - Mid 5 pair

4 = Mid 6 - Mid 7 pair

5 = Mid 8 - Mid 9 pair

6 = Mid 10 - Mid 11 pair

7 = Mid 12 - Mid 13 pair

8 = Mid 14 - Bottom pair

***Net number*** Defines the net to which the primitive is attached in the attached netlist. All net numbers are assigned sequentially in the order that the net is listed in the netlist section of the PCB

file. A primitive that is attached to net number 1 is attached to the first net listed in the netlist section (1-32768).

***Net reconnect*** Defines the optimization method used to order connections in the attached netlist. Range of values include:

0 = x-Bias
1 = y-Bias
2 = Shortest
3 = Daisy Chain
4 = Min Daisy Chain
5 = Start/End Daisy

***Plane*** Defines the connection of a pin to any of the plane layers (0-12).

0 = no plane connection
1 = relief to plane 1
2 = direct to plane 1
3 = tagged to plane 1
4 = relief to plane 2
5 = direct to plane 2
6 = tagged to plane 2
7 = relief to plane 3
8 = direct to plane 3
9 = tagged to plane 3
10 = relief to plane 4
11 = direct to plane 4
12 = tagged to plane 4

***Routed by*** Identifies the pass used to route a connection in the attached netlist (1-7).

1 = PreRouter
2 = SmdStringers
3 = Memory Router
4 = Line Probe
5 = Maze
6 = Smoother
7 = Arc Replacer

***Source*** Special node (or pin) definition in netlists, used to indicate the first or center node in a net, depending upon the optimization topology.

***Start angle*** Defines the beginning angle of an arc (in degrees) where the 3 o'clock position from the arc center is 0 degrees. The angle is measured in a counter-clockwise rotation, so that a start angle at the 12 o'clock position would be 90 (0.001-360.000).

***Terminator*** 1. Special node (or pin) definition in netlists, used to indicate the last or end node in a net, depending upon the optimization topology. 2. Special pad type definition used to indicate the end of the routed portion of a partially routed connection.

## Advanced PCB files

The following files are delivered with Advanced PCB:

***PFW.EXE***

The main (or *executable)* Advanced PCB application.

***PFW.PAD***

This is the default set of pad type definitions. Advanced PCB will search for this at start up. If not found then no components or pads will be placed when files are loaded. To change the default set, simply save your set of pad type definitions to the file PFW.PAD.

***PFW.LIB***

The default library of patterns for components on the PCB. Advanced PCB will search for this at start up. If this file is not found at start-up, no components will be placed until another library is specified.

***PFW.HLP***

This file is the Advanced PCB on-line help system. If it is in the same directory as PFW.EXE, it will be loaded automatically when you use the Help menu commands (or press the Help button or F1).

***README.TXT***

This file contains release notes for the current (shipping) version of Advanced PCB. An option to view this file is automatically presented during installation of the software.

***PFW.XRF***

This text file is a cross reference between over 6500 standard OrCAD SDT library component names and the patterns listed in the PFW.LIB file. When loading an OrCAD netlist (Netlist-Load command), these patterns are automatically placed in the PCB workspace. OrCAD SDT 4 users need

only generate the netlist using the “Tango” format for this feature to work. The .XRF file is a simple ASCII text file which can be edited by the user. The component name (comment field ) is listed first, then the Advanced PCB library pattern. Multiple patterns can be included for each component name. The first pattern is the default. If this pattern is not in the current library, the next pattern will be accepted, and so on. The cross-referencing is intelligent – for example, it will parse the nearest name from partially matched strings (e.g. DIL14 will be parsed as DIP14).

### Other supplied files

The following demonstration files are supplied:

| | |
|---|---|
| DEMO1.PCB | This is a small through-hole layout, in placed but unrouted condition. You can use this board to demonstrate various auto place and router options. |
| DEMO1.NET | The netlist for DEMO1.PCB and DEMOSMD.PCB. You can use this netlist to demonstrate auto placement, autorouting and DRC features of the system. |
| DEMO2.PCB | This is a larger through-hole layout in placed but unrouted condition. |
| DEMO2.NET | The netlist for DEMO2.PCB. |
| DEMO1.NET | The netlist for DEMO1.PCB and DEMOSMD.PCB. You can use this netlist to demonstrate auto placement, autorouting and DRC features of the system. |
| DEMO1AP.PCB | Auto placed version of DEMO1. |

DEMO2AP.PCB Auto placed version of DEMO2.

Files listed below are created as you work with Advanced PCB:

***(filename).PCB***

Used to store a PCB layout or exported selection from the current board file (File-Export Selection command).

Settings that are saved with PCB file, with their (default) settings:

Top layer (On)
Bottom layer (On)
Top Overlay layer (On)
Multi-layer (On)
Keep Out layer (On)
Highlight layer (On)
DRC Error layer (On)
Grid color1 (On)
Internal plane1 (On)
Internal plane2 (On)
Rats Nest layer (On)
All others (Off)
Visible grid-1 (25)
Visible grid-2 (100)
Snap grid (25)
Current layer (Top layer)
Scroll bars (On)
Tool bar (On)

***(filename).NET***

Protel format (ASCII) netlist file. Two formats are supported: Protel and Protel2, both identified by the extension ".NET."

***(filename).RPT***

a text report file of netlist contents.

***(filename).LOG***

report of autorouting results, including passes run, completion rates and primitives counts.

***(filename).MAT***

text file that records Gerber aperture assignments.

***PCB.DMP***

text file of any Information window list.

***(filename).DRC***

Design rule check result file in ASCII text format.

***(filename).BOM***

Bill of material files generated by Advanced PCB.

***(filename).AB0, AB1, etc.***

Automatic backups for PCB files, generated on a rotating basis. The most recent version is loaded when the File-Restore Backup command is used.

***(filename).ECO***

Engineering Change Order (.ECO) files support forward and backward annotation of PCBs and schematics. Changes are recorded in user-editable ASCII text. The format used is identical (and compatible with) the format used by PADS-PCB™ and PADS2000™. The format is:

```
*PADS-ECO*
```

Header of .ECO file.

```
*NET*
*SIGNAL*  CLOCK2  12
```

Adds a node to the net CLOCK2, indicating a track width of 12 mils.

```
U1.8  U13.16  R1
```

Nodes (pins) associated with this net.

```
*SIGNAL*  VDD  100
R1.2  U1.1  U2.1  U3.1
```

Adds a new net named VDD, and its associated pins.

```
*JOINNET*
VCC VDD
```

Joins two nets named VCC and VDD. VDD is assigned as identifier.

```
*DELPIN*
R12.22   COM
```

Deletes a pin from a net. The net name is optional.

```
*SPLITNET*
*SIGNAL* RND
U21.7  N2.2  U4.16
*SIGNAL* RND2
U29.3  N3.2  U11.4  X1.1
```

Splits an existing net (RND) into two nets by adding the new net (RND2) and listing its nodes.

```
*RENNET*
A00  RESET
```

Renames the net A00 to Reset.

```
*PART*
U1  74LS02
```

Adds a new unplaced, unconnected part to the design.

*DELPART*
U1 74LS00

Removes a part from the design.

*RENPART*
U1 U23
U7 U24

Re-annotates specified parts.

*CHGPART*
74LS00 74LS02

Changes the part type (comment field).

*SWPGAT*
*SWPPIN*

Swap gate and swap pin information. This data is currently ignored by Protel.

*REMARK*

Header for any information added by user.

*END*

End-off-file marker.

### PFW.INI

This file (written to the Windows directory) stores current system-level defaults from one session to another. This file is created the first time you run Advanced PCB and re-written (using the current settings and preferences), each time you Exit from the program. If you want to temporarily re-set all defaults back to their original settings or have several default set-ups for different projects, then temporarily re-name the PFW.INI file. Some settings are stored as part of the .PCB document (see below).

Many of the options that are saved are listed below (default settings are in parentheses). Other internal system settings are also saved. The .INI file can be examined or modified using a text editor. Each entry is identified by a name (in

brackets), proceeding the data field. The user can, if desired, directly manipulate the file contents, providing that care is taken to preserve its syntax and ASCII-only content. No hidden characters (such as word processor line feeds) are allowed.

### *Printer Options*

Show Holes (Off)
Scale To Fit Page (Off)
Use Software Arcs (On)
Use Printer Fonts (Off)
Batch Type (Color Composite)
Scale (1.0)
XCorrect (1.0)
YCorrect (1.0)
Border Size (1000)

### *Gerber Options*

Use Software Arcs (On)
Plus Tolerance (0)
Minus Tolerance (2)
Film Size X (20000)
Film Size Y (16000)
Border Size (1000)
Vector Plotter Sort (On)
Batch Mode (Panelize)
G54 With aperture (Off)

### *Output Options (Shared Print & Gerber)*

Drill Guide Hole Size (30)
Drill Draw Symbol Size (50)
Relief Conductor Width (20)
Relief Air Gap (10)
Solder Mask Expansion (5)
Paste Mask Expansion (0)
Power Plane Expansion (5)
All Flip Layers (Off)

### *Component Comment Defaults*

Size (60)

Rotation (Horizontal)
Layer (Overlay)
Show/Hide (Show)
Font (Default)
Vertical Align (Top)
Horizontal Align (Left)

### *Component Designator Defaults*

Size (60)
Rotation (Horizontal)
Layer (Overlay)
Show/Hide (Show)
Font (Default)
Vertical Align (Top)
Horizontal Align (Left)
Global System Options
PlaceTrackMode (Linear45)
Current Track Width (12)
Current String Size (60)
Current Via Size (50)
Current Via Hole Size (28)
Current String Font (Default)
Lock physical to logical cursor (on)
Transparent Colors (Off)
Dithered Colors (Off)
Pad Numbers (On)
Pad Nets (On)
Drag tracks with comp move (On)
Display Modes (Full for all primitives)
Auto Backup File Name (FileName.AB0–9)
Auto Backup Time (30)
Auto Via (On)
Place Via Type (Normal)
Question Delete (Off)
Auto Pan (On)
Cursor Type (Small 90 Cross)

### Array Place Options

Count (1)
Degrees (45)
Linear/Circular (Linerar)
X-offset (1000)
Y-offset (0)
Increment (1)

### Autorouter Options

Route Passes (On)
- Memory
- Line Probe
- Maze

Route Passes (Off)
- Pre-Route
- SMD Stringers
- Smoother
- Arc Replace

GridSize (25)
TrackSize (12)
ViaSize (50)
Maze/Smooth Passes (5)
Top Layer (Vertical)
Bottom Layer (Horizontal)
All others (Not Used)
Route Hugging before 100% (Hug)
Route Hugging after 100% (Spread)
Route With Blind/Buried Vias (Off)

### Autoplace Options

Grid (100)
Large Clear (100)
Small Clear (50)
Use Grouping (On)
Global/Local (Global
Allow Rotation (Off)
BypassNet1 (None)
BypassNet2 (None)
Shove Depth (2)

### DRC Settings

**(All options turned on by default)**

Missing Component Errors
Missing Pin Errors
Extra Pin Errors
Extra UnNamed Pin Errors
Split Net Errors
Clearance Errors
Extra Net Errors
Extra Component Errors
Pattern Errors
Component Value Errors
Make DRC File
Make DRC Error List

## .PIK file format

This report format supports programming of pick-and-place equipment, used to insert components into the fabricated PCB. The user can produce this report in two formats, ASCII text or in CSV (comma separated value) format, which can be loaded into a database or spreadsheet.

| Designator | Pattern | Coordinates (x, y) | | Status | Rotation |
|---|---|---|---|---|---|
| U6 | DIP40 | 4700mil | 3590mil | T | 0.000 |
| U7 | DIP40 | 5420mil | 3590mil | T | 0.000 |
| J4 | IDC40P | 5950mil | 3270mil | T | 180.000 |
| C7 | RB.2/.4 | 6060mil | 1380mil | T | 270.000 |
| SW1 | CHR1.0 | 5370mil | 1350mil | L | -99.000 |
| U12 | DIP16 | 5370mil | 1810mil | T | 270.000 |
| R6 | AXIAL0.4 | 4420mil | 2300mil | B | 270.000 |
| U1 | DIP14 | 4150mil | 2220mil | T | 180.000 |
| N0 | TPX | 4750mil | 1520mil | P | -99.000 |

Coordinates represent the component center, derived from pad locations. Status variables: T (Top layer); B (Bottom layer); L (no library information); P (single pad). All libraries used in the board must be loaded when generating a .PIK report. Un-supported components indicate -99.000 rotation.

## Print / Plot file extensions

If you have directed the output to a file, and intend to use the services of a plotting bureau, use of standardized extensions to identify each plot layer is highly recommended. The following extensions are automatically generated by Advanced PCB:

| | | | |
|---|---|---|---|
| Check plot | .PCK | Power planes 1-4 | .PP* |
| Top layer | .PTL | Mechanical 1-4 | .PF* |
| Mid layer 1-14 | .PM* | Top Solder mask | .PTS |
| Keep Out layer | .PKO | Bottom Solder mask | .PBS |
| DRC layer | .PDR | Drill guide | .PDG |
| Bottom layer | .PBL | Drill drawing | .PDD |
| Top overlay | .PTO | Bottom overlay | .PBO |
| Top Paste mask | .PTP | Bottom Paste mask | .PBP |

Advanced PCB uses a similar scheme for identifying print files. In this case the letter “R” is substituted for “P.”

## Identifying Gerber plot files

Gerber plot filenames are automatically appended with a unique extension that identifies layer and plot type. For example, the Top layer plot of a file called “TEST” will be saved as “TEST.GTL,” to indicate “Gerber-Top layer.” Because each design can generate several plot files, these tags help identify “sets” of output files.

➡ Using a unique extension for different layers and file types allows you to retain a common filename (e.g. TEST) to simplify identification later.

We recommend that you follow this convention which conforms to general industry practice.

| | | | |
|---|---|---|---|
| Top overlay | .GTO | Bottom layer | .GBL |
| Top layer | .GTL | Power plane 1, etc. | .GP1 |
| Mid layer 1, etc. | .GM1 | Top Solder mask | .GTS |
| Mechanical layer 1 | .GF1 | Bottom Solder mask | .GBS |
| Drill drawing | .GDD | Pad master | .GPM |
| Drill guide | .GDG | Keep Out layer | .GKO |

## NC drill files

The File-NC Drill command generates the following three files for each fabrication layer:

An Excellon format file with the extension .DRL, DR1, DR2, etc. (this is the binary Excellon format file);

A report file (.DRR) is generated listing the number of holes for each drill and the size in both metric and imperial measurement;

An ASCII version of the binary file with the extension (.TXT, TX1, TX2, etc).This file is used to verify the contents of the binary version. Use the Windows Notepad (or other text editor / word processor to open and view this file.

If there are blind or buried vias in the design, Advanced PCB will generate additional drill files with modified extensions that identify each layer pair. For example, a board with four signal layers and blind/buried vias will produce three different NC drill file sets.

The drill control file (Extension DRL, DR1, etc.) is written in the EIA character (binary) format in the EXCELLON language. The data is specified in mils (.001 in) with trailing zeros suppressed. Drill tools are numbered from 1– 255.

The extensions are:

Top - Bottom (Though hole)..... TXT and DRL
Top - Mid layer 1 ..... TX1 and DR1
Mid layer 2 - Mid layer 3 ..... TX2 and DR2
Mid layer 4 - Mid layer 5 ..... TX3 and DR3
Mid layer 6 - Mid layer 7 ..... TX4 and DR4
Mid layer 8 - Mid layer 9 ..... TX5 and DR5
Mid layer 10 - Mid layer 11 ..... TX6 and DR6
Mid layer 12 - Mid layer 13 ..... TX7 and DR7
Mid layer 14 - Bottom..... TX8 and DR8

### Report file (.DRR)

The drill report file (.DRR) is supplied in the following format. You can view this report directly from Windows by using the Notepad feature. Just change the extension mask in Notepad to .DRR to open the file.

NC Dill File Report For : C:\PFW\TEST.PCB 30-Aug-1991 11:53:11

| Tool | Hole Size | Hole Count | Tool Travel |
|---|---|---|---|
| T1 | 30 Mil (0.750 mm) | 422 | 73.30 Inch (1861.90 mm) |
| Totals | | 422 | 73.30 Inch (1861.90 mm) |

Total Processing Time: 00:00:09

### The ASCII (.TXT) report

In this example M48 is the Excellon format header and % is a standard tape rewind instruction. The file then lists the

tools used, followed by the coordinates for each hole assigned to that tool.

Note that the unchanged x coordinate is ignored in the sample. These coordinates differ from the standard Autotrax numeric format. All trailing zeros are suppressed (deleted) e.g. 3.50 inches is displayed 035 and 18.555 inches is displayed as 18555.

```
M48
    T1F00S00
%
T01
    X00225Y00725
    X00425
    X04525Y00675
    (etc)
```

### DRC report file format

An extract from a DRC report follows, showing the possible error and warning messages:

Net C9.2_U9.11 Broken Into 2 Sub-Nets

Sub-Net 1

C9-2

Sub-Net 2

U9-11 R4-1

Component Missing From PCB : C10

Extra Pin On Net CPUCLK : U3-22

Extra Pin On Net CPUCLK : U3-26

Clearance Error On Net : CPUCLK

Track (4225,3325 4299,3576) Bottom Layer

Track (4325,3425 4325,3625) Bottom Layer

# Tools and shortcuts

## Toolbar

The Tool bar provides convenient button access to the most commonly used menu commands. The Tool bar can be hidden, if preferred (Options menu). For detailed descriptions of tools, see the Commands section of this reference.

Tool button command assignments are:

| | |
|---|---|
| *File-Open* | *Edit-Place-Component* |
| *File-Save* | *Edit-Place-Fill* |
| *File-Print* | *Edit-Place-Pad* |
| *Zoom-All* | *Edit-Place-String (text)* |
| *Zoom-Window* | *Edit-Place-Track* |
| *Zoom-Redraw* | *Edit-Place-Via* |
| *Edit-Cut (selection)* | *Edit-Place-Array* |
| *Edit-Paste (clipboard)* | *Library-Components* |
| *Edit-Select-Inside Area* | *File-Run Schematic Capture* |
| *Edit-DeSelect-All* | *Edit-Undo* |
| *Edit-Move-Move Selection* | *Edit-Redo* |
| *Current-Snap Grid* | *Help (Contents)* |
| *Edit-Place-Arc (center)* | |

## Mouse and keyboard shortcuts

Two sets of keystroke shortcuts are available: standard Windows combinations of the ALT key and a command key (underscored in the menu). For example, press ALT, F to

open the File menu. A second set of Protel default shortcuts augments these options, for example, to open the File menu, just press F once. Other shortcuts include:

| | |
|---|---|
| ALT, F or F | File menu |
| ALT, E | Edit menu |
| ALT, L or L | Library menu |
| ALT, M or M | NetList menu |
| ALT, A or A | Auto menu |
| ALT, C or C | Current menu |
| ALT, O or O | Options menu |
| ALT, Z or Z | Zoom menu |
| ALT, I or I | Info menu |
| ALT, W or W | Window menu |
| ALT, H or H | Help menu |
| ALT+BACKSPACE | Undo |
| E | Edit-Change menu |
| U | Auto-Placement Tools menu |
| T | Edit-Toggle Selection menu |
| X | Edit-De-Select menu |
| CTRL+A | Edit-Place Arc (Center) |
| CTRL+G | Current-Snap Grid |
| CTRL+H | Edit-Select-Physical Net |
| CTRL+L | Current-Layer |
| CTRL+M | Info-Measure Distance |
| CTRL+P | Library-Pad |
| CTRL+S | Current-Free Text-Height |
| CTRL+T | Current-Track (width) |

| | |
|---|---|
| CTRL+U | Un-delete one item |
| CTRL+V | Current Via Size |
| CTRL+Z | Zoom Window |
| PGUP | Zoom Expand |
| PGDN | Zoom Contract |
| CTRL+PGUP/PGDN | Zoom maximum / minimum |
| SHIFT+PGUP/PGDN | Zoom at 0.1 step rate |
| HOME | Zoom Pan |
| END | Zoom Redraw |
| CTRL+HOME | Jump Absolute Origin |
| CTRL+END | Jump Relative Origin |
| CTRL+INS | Edit-Copy |
| CTRL+DEL | Edit-Clear |
| SHIFT+INS | Edit-Paste |
| SHIFT+DEL | Edit-Cut |
| SHIFT+F4 | Cascade Windows |
| SHIFT+F5 | Tile Windows |
| * | Toggle active signal layers |
| + or - | Next / previous active layer |
| F1 | Help Index |
| UP, DOWN, | Move one snap grid point, vertically |
| SHIFT+UP, DOWN, | Move 10 snap grid points, vertically |
| LEFT, RIGHT | Move one snap grid point, horizontally |
| SHIFT+LEFT, RIGHT | Move 10 snap grid points, horizontally |

### Special mode-dependent keys

| | |
|---|---|
| SPACEBAR | Toggle track placement modes; rotates item during selection or move (uses |

preset step value in Options-Preference dialog box); aborts screen redraw.

TAB — Opens current menu to assign new value when placing arcs, pads, strings, tracks or vias.

SHIFT — When placing or moving items, pans at 5x the normal rate.

### Special strings

The following pre-defined strings can be placed on any layer of your artwork for plotting. If you place these strings on the Multi layer, they will be printed/plotted on each layer sheet. For example, .DATE_PRINT will automatically place the current date (from the system clock) as the file is printed or generated.

| | |
|---|---|
| .DATE_PRINT | .TRACK_COUNT |
| .TIME_PRINT | .PAD_COUNT |
| .LAYER.NAME | .VIA_COUNT |
| .PLOT_FILE_NAME | .FILL_COUNT |
| .PCB_FILE_NAME | .COMPONENT_COUNT |
| .STRING_COUNT | .NET_COUNT |
| .HOLE_COUNT | .LEGEND |

The LEGEND option generates a drill drawing-style legend with hole sizes and counts for the board. All Special strings can be rotated or mirrored, like normal strings.

### Need more information?

Please check both the On-line Help system and the README.TXT document (use the Windows Notepad utility to view and/or print this file). Both of these information sources include updated/expanded information about Advanced PCB.

# Library components

➡ ***Important*** The following component information is provided for reference only. It is not intended to replace manufacturer's databooks. Because of the large amount of information, there is always the possibility of errors or omissions in the documentation or in the library patterns. Final responsibility for design integrity remains with the user. We strongly recommend that all designers adhere to standard industry practice in carefully checking all artwork before committing any design to production.

## Through-hole component patterns

| Pattern | Pins | Description | Dimensions | |
|---|---|---|---|---|
| AXIAL0.3 | 2 | Axial device | .3 in. pin spacing | |
| AXIAL0.4 | 2 | | .4 in. pin spacing | |
| AXIAL0.5 | 2 | | .5 in. pin spacing | |
| AXIAL0.6 | 2 | | .6 in. pin spacing | |
| AXIAL0.7 | 2 | | .7 in. pin spacing | |
| AXIAL0.8 | 2 | | .8 in. pin spacing | |
| AXIAL0.9 | 2 | | .9 in. pin spacing | |
| AXIAL1.0 | 2 | | 1.0 in. pin spacing | |
| DIODE0.4 | 2 | Axial diode | .4 in. pin spacing | |
| DIODE0.7 | 2 | | .7 in. pin spacing | |
| POLAR0.6 | 2 | Axial electrolytic cap | .6 in. pin spacing | |
| POLAR0.8 | 2 | | .8 in. pin spacing | |
| POLAR1.0 | 2 | | 1.0 in. pin spacing | |
| POLAR1.2 | 2 | | 1.2 in. pin spacing | |
| RB.2.4 | 2 | Radial lead electrolytic cap | .2 in. pin spacing | .4 in. diameter |
| RB.3.6 | 2 | | .3 in. pin spacing | .6 in. diameter |
| RB.4.8 | 2 | | .4 in. pin spacing | .8 in. diameter |
| RB.51.0 | 2 | | .5 in. pin spacing | 1.0 in. diameter |
| RAD0.1 | 2 | Radial cap | .1 in. pin spacing | |
| RAD0.2 | 2 | | .1 in. pin spacing | |
| RAD0.3 | 2 | | .1 in. pin spacing | |
| RAD0.4 | 2 | | .1 in. pin spacing | |

| | | |
|---|---|---|
| TO-3 | 3 (4) | Jedec outline transistor |
| TO-5 | 3 | |
| TO-18 | 3 | |
| TO-39 | 3 | |
| TO-46 | 3 | |
| TO-52 | 3 | |
| TO-66 | 3 (4) | |
| TO-72 | 4 | |
| TO-92A | 3 | |
| TO-92B | 3 | |
| TO-126 | 3 | |
| TO-220 | 3 (4) | |
| FUSE | 1 | fuse holder |
| HEPTA | 9 | |
| MULTI11 | 11 | |
| MULTI15 | 15 | |
| PENTA | 7 | |
| VR1 | 3 | variable res |
| VR2 | 3 | |
| VR3 | 3 | |
| VR4 | 3 | |
| VR5 | 3 | |
| XTAL1 | 2 | crystal |
| BNC | 2 (5) | BNC conn |
| DB9F | 9 | female conn |
| DB9M | 9 | male conn |
| DB9RAF | 9 | right angle female conn |
| DB9RAM | 9 | right angle female conn |
| DB15F | 15 | female conn |
| DB15M | 15 | male conn |
| DB15RAF | 15 | right angle female conn |
| DB15RAM | 15 | right angle male conn |
| DB25F | 25 | female conn |
| DB25M | 25 | male conn |
| DB25RAF | 25 | right angle female conn |
| DB25RAM | 25 | right angle male conn |
| DB37F | 37 | female conn |
| DB37M | 37 | male conn |
| DB37RAF | 37 | right angle female conn |
| DB37RAM | 37 | right angle male conn |
| DIN96 | 96 | DIN conn |
| DIN96RA | 96 | right angle DIN connector |

| | | | | |
|---|---|---|---|---|
| FLY4 | 4 | conn | | |
| IDC10 | 10 | Insulation disp. conn | | |
| IDC16 | 16 | | | |
| IDC20 | 20 | | | |
| IDC26 | 26 | | | |
| IDC34 | 34 | | | |
| IDC36 | 36 | | | |
| IDC40 | 40 | | | |
| IDC40P | 40 | | | |
| IDC50 | 50 | | | |
| IDC50P | 50 | | | |
| POWER4 | 4 | power conn | | |
| POWER6 | 6 | | | |
| SPADE | 1 | spade conn | | |
| SIP2 | 2 | single inline pack | 100 mil pin spacing | |
| SIP3 | 3 | | 100 mil pin spacing | |
| SIP4 | 4 | | 100 mil pin spacing | |
| SIP5 | 5 | | 100 mil pin spacing | |
| SIP6 | 6 | | 100 mil pin spacing | |
| SIP7 | 7 | | 100 mil pin spacing | |
| SIP8 | 8 | | 100 mil pin spacing | |
| SIP9 | 9 | | 100 mil pin spacing | |
| SIP10 | 10 | | 100 mil pin spacing | |
| SIP12 | 12 | | 100 mil pin spacing | |
| SIP16 | 16 | | 100 mil pin spacing | |
| SIP20 | 20 | | 100 mil pin spacing | |
| DIP4 | 4 | dual inline pack | 100 mil pin spacing | 300 mil row spacing |
| DIP6 | 6 | | 100 mil pin spacing | 300 mil row spacing |
| DIP8 | 8 | | 100 mil pin spacing | 300 mil row spacing |
| DIP14 | 14 | | 100 mil pin spacing | 300 mil row spacing |
| DIP16 | 16 | | 100 mil pin spacing | 300 mil row spacing |
| DIP18 | 18 | | 100 mil pin spacing | 300 mil row spacing |
| DIP20 | 20 | | 100 mil pin spacing | 300 mil row spacing |
| DIP22 | 22 | | 100 mil pin spacing | 400 mil row spacing |
| DIP24 | 24 | | 100 mil pin spacing | 600 mil row spacing |
| DIP28 | 28 | | 100 mil pin spacing | 600 mil row spacing |
| DIP32 | 32 | | 100 mil pin spacing | 600 mil row spacing |
| DIP40 | 40 | | 100 mil pin spacing | 600 mil row spacing |
| DIP48 | 48 | | 100 mil pin spacing | 600 mil row spacing |
| DIP52 | 52 | | 100 mil pin spacing | 600 mil row spacing |
| DIP64 | 64 | | 100 mil pin spacing | 600 mil row spacing |

| | | | | |
|---|---|---|---|---|
| QUIL64 | 64 | quad inline pack | 100 mil pin spacing | |
| PGA52X9 | 52 | pin grid array | 100 mil pin spacing | 9x9 rows |
| PGA64X10 | 64 | | 100 mil pin spacing | 10x10 rows |
| PGA68X10 | 68 | | 100 mil pin spacing | 10x10 rows |
| PGA68X11 | 68 | | 100 mil pin spacing | 11x11 rows |
| PGA84X10 | 84 | | 100 mil pin spacing | 10x10 rows |
| PGA84X11 | 84 | | 100 mil pin spacing | 11x11 rows |
| PGA84X12 | 84 | | 100 mil pin spacing | 12x12 rows |
| PGA84X13 | 84 | | 100 mil pin spacing | 13x13 rows |
| PGA88X13 | 88 | | 100 mil pin spacing | 13x13 rows |
| PGA100X10 | 100 | | 100 mil pin spacing | 10x10 rows |
| PGA114X13 | 114 | | 100 mil pin spacing | 13x13 rows |
| PGA120X13 | 120 | | 100 mil pin spacing | 13x13 rows |
| PGA124X13 | 124 | | 100 mil pin spacing | 13x13 rows |
| PGA132X13 | 132 | | 100 mil pin spacing | 13x13 rows |
| PGA179X18 | 179 | | 100 mil pin spacing | 18x18 rows |
| PGA208X17 | 208 | | 100 mil pin spacing | 17x17 rows |
| CAN8 | 8 | multi-pin analog dev | | |
| CAN10 | 10 | | | |
| CAN12 | 12 | | | |

## SMD component patterns

| Pattern | Pins | Description | Dimensions | |
|---|---|---|---|---|
| LCC16 | 16 | Leadless chip carrier | 50 mil pin spacing | 100x24 pads |
| LCC18 | 18 | | 50 mil pin spacing | 100x24 pads |
| LCC18ECA | 18 | (Jedec ECA pack) | 50 mil pin spacing | 100x24 pads |
| LCC18ECB | 18 | (Jedec ECB pack) | 50 mil pin spacing | 100x24 pads |
| LCC20 | 20 | | 50 mil pin spacing | 100x24 pads |
| LCC20ECD | 20 | (Jedec ECD pack) | 50 mil pin spacing | 100x24 pads |
| LCC24 | 24 | | 50 mil pin spacing | 100x24 pads |
| LCC28 | 28 | | 50 mil pin spacing | 100x24 pads |
| LCC32 | 32 | | 50 mil pin spacing | 100x24 pads |
| LCC44 | 44 | | 50 mil pin spacing | 100x24 pads |
| LCC52 | 52 | | 50 mil pin spacing | 100x24 pads |
| LCC68 | 68 | | 50 mil pin spacing | 100x24 pads |
| LCC84 | 84 | | 50 mil pin spacing | 100x24 pads |
| LCC100 | 100 | | 50 mil pin spacing | 100x24 pads |
| LCC124 | 124 | | 50 mil pin spacing | 100x24 pads |
| LCC150 | 150 | | 50 mil pin spacing | 100x24 pads |
| LCCC68 | 68 | J-leaded Cerdip chip carrier | 50 mil pin spacing | 100x24 pads |
| LCCC84 | 84 | | 50 mil pin spacing | 100x24 pads |

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|---|---|---|---|---|
| PLCC18 | 18 | Plastic J-leaded chip carrier | 50 mil pin spacing | 75x24 pads |
| PLCC18L | 18 | | 50 mil pin spacing | 75x24 pads |
| PLCC20 | 20 | | 50 mil pin spacing | 75x24 pads |
| PLCC22 | 22 | | 50 mil pin spacing | 75x24 pads |
| PLCC28 | 28 | | 50 mil pin spacing | 75x24 pads |
| PLCC28R | 28 | | 50 mil pin spacing | 75x24 pads |
| PLCC32 | 32 | | 50 mil pin spacing | 75x24 pads |
| PLCC44 | 44 | | 50 mil pin spacing | 75x24 pads |
| PLCC52 | 52 | | 50 mil pin spacing | 75x24 pads |
| PLCC68 | 68 | | 50 mil pin spacing | 75x24 pads |
| PLCC84 | 84 | | 50 mil pin spacing | 75x24 pads |
| PLCC100 | 100 | | 50 mil pin spacing | 75x24 pads |
| PLCC124 | 124 | | 50 mil pin spacing | 75x24 pads |
| PJLCC28 | 28 | JEDIC J-leaded PLCC | 50 mil pin spacing | 80x24 pads |
| PJLCC44 | 44 | | 50 mil pin spacing | 80x24 pads |
| PJLCC52 | 52 | | 50 mil pin spacing | 80x24 pads |
| PJLCC68 | 68 | | 50 mil pin spacing | 80x24 pads |
| PJLCC84 | 84 | | 50 mil pin spacing | 80x24 pads |
| PJLCC100 | 100 | | 50 mil pin spacing | 80x24 pads |
| PJLCC124 | 124 | | 50 mil pin spacing | 80x24 pads |
| PJLCC156 | 156 | | 50 mil pin spacing | 80x24 pads |
| ILEAD8 | 8 | I-leaded dual inline pack | 100 mil pin spacing | 100x50 pads |
| ILEAD14 | 14 | | 100 mil pin spacing | 100x50 pads |
| ILEAD16 | 16 | | 100 mil pin spacing | 100x50 pads |
| ILEAD18 | 18 | | 100 mil pin spacing | 100x50 pads |
| ILEAD20 | 20 | | 100 mil pin spacing | 100x50 pads |
| ILEAD22 | 22 | | 100 mil pin spacing | 100x50 pads |
| ILEAD24 | 24 | | 100 mil pin spacing | 100x50 pads |
| ILEAD28 | 28 | | 100 mil pin spacing | 100x50 pads |
| 3216 | 2 | Tantalum cap IPC-SM-782 | 3.2x1.6 mm | |
| 3518 | 2 | | 3.5x1.8 mm | |
| 3527 | 2 | | 3.5x2.7 mm | |
| 3528 | 2 | | 3.5x2.8 mm | |
| 6032 | 2 | | 6.0x4.3 mm | |
| 7227 | 2 | | 7.2x2.7 mm | |
| 7243 | 2 | | 7.2x4.3 mm | |
| 7257 | 2 | | 7.2x5.7 mm | |
| SOT-23 | 3 | Sm outline trans IPC-SM-782 | | |
| SOT-25 | 5 | | | |
| SOT-89 | 3 | | | |
| SOT-143 | 4 | | | |

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|---|---|---|---|---|
| 0402 | 2 | Chip res/cap IPC-SM-782 | 40x20 mil | |
| 0603 | 2 | | 60x30 mil | |
| 0805 | 2 | | 80x50 mil | |
| 1005 | 2 | | 100x50 mil | |
| 1206 | 2 | | 120x60 mil | |
| 1210 | 2 | | 120X100 mil | |
| 1805 | 2 | | 180x50 mil | |
| 1808 | 2 | | 180x80 mil | |
| 1812 | 2 | | 180x125 mm | |
| 1825 | 2 | | 180X250 mil | |
| 2220 | 2 | | 220x200 mil | |
| 2225 | 2 | | 220x250 mil | |
| QFP44 | 44 | Quad plastic flat pack (st lead) | 14.5x13.5 mm body | 100x16 mil pads on .8 mm ctrs |
| QFP44-1 | 44 | | 12.3x12.3 mm | 75x16 mil pads on .8 mm |
| QFP44-2 | 44 | | 12.3x12.3 mm | 75x16 mil pads on .8 mm |
| QFP44-2 | 44 | | 12.3x12.3 mm | 75x16 mil pads on .8 mm |
| QFP44-3 | 44 | | 14.4x14.4 mm | 95x16 mil pads on .8 mm |
| QFP48 | 48 | | 17.3x17.3 mm | 110x16 mil pads on .8 mm |
| QFP52 | 52 | | 21.3x21.3 mm | 110x20 mil pads on 1.0 mm |
| QFP54 | 54 | | 14.4x14.4 mm | 80x13 mil pads on .65 mm |
| QFP56 | 56 | | 13.5x14.5 mm | 80x16 mil pads on .65 mim |
| QFP56-2 | 56 | | 24x20 mm | 80x20 mil pads on 1.0 mm |
| QFP60 | 60 | | 24x20 mm | 80x20 mil pads on 1.0 mm |
| QFP64 | 64 | | 17.6x17.6 mm | 100x20 mil pads on 1.0 mm |
| QFP64-1 | 64 | | 17.6x17.6 mm | 75x16 mil pads on .8 mm |
| QFP64-2 | 64 | | 18.7x24.7 mm | 75x20 mil pads on 1.0 mm |
| QFP64-3 | 64 | | 18.4x18.4 mm | 80x16 mil pads on .8 mm |
| QFP64-4 | 64 | | 18.7x24.7 mm | 90x20 mil pads on 1.0 |
| QFP64-5 | 64 | | 22.8x22.8 mm | 400x25 mil pads on 50 mil |
| QFP70 | 70 | | 16.4x28.7 mm | 120x16 mil pads on .8 mm |
| QFP74 | 74 | | 23.2x23.2 mm | 75x20 mil pads on 1.0 mm |
| QFP80-1 | 80 | | 14x14 mm | 75x13 mil pads on .65 mm |
| QFP80-2 | 80 | | 14x20 mm | 75x16 mil pads on .8 mm |
| QFP88 | 88 | | 14x20 mm | 75x13 mil pads on .8 mm |
| QFP90 | 90 | | 14x20 mm | 100x16 mil pads on .8 mm |
| QFP94 | 94 | | 23.2x23.2 mm | 75x16 mil pads on .8 mm |
| QFP100 | 100 | | 20x5x14 mm | 75x12 mil pads on .65 mm |
| QFP100-2 | 100 | | 19.5x14 mm | 75x13 mil pads on .65 mm |
| QFP120 | 120 | | 32x32 mm | 75x16 mil pads on .8 mm |
| QFP128 | 128 | | 28x28 mm | 75x16 mil pads on .8 mm |
| QFP136 | 136 | | 28x28 mm | 75x13 mil pads on .65 mm |
| QFP144 | 144 | | 28x28 mm | 75x13 mil pads on .65 mm |
| QFP160 | 160 | | 28x28 mm | 75x13 mil pads on .65 mm |
| QFP196 | 196 | | 32.5x232.5 mm | 75x13 mil pads on .65 mm |

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|---|---|---|---|
| MLL34 | 2 | Tubular pack IPC-SM-782 | |
| MLL41 | 2 | | |
| MELF1 | 2 | Metal elec faced IPC-SM-782 | |
| MELF2 | 2 | | |
| TAPE84-15 | 84 | 35 mm Tape Automatic bonded comp | 75x8 mil pads on 15 mil centers |
| TAPE84-20 | 84 | 35 mm | 75x12 mil pads on 20 mil |
| TAPE100-20 | 100 | 35 mm | 75x12 mil pads on 20 mil |
| TAPE124-10 | 124 | 35 mm | 75x5 mil pads on 10 mil |
| TAPE132-15 | 132 | 35 mm | 75x8 mil pads on 15 mil |
| TAPE140-20 | 140 | 35 mm | 75x12 mil pads on 20 mil |
| TAPE180-20 | 180 | 48 mm | 75x12 mil pads on 20 mil |
| TAPE188-15 | 188 | 35 mm | 75x8 mil pads on 15 mil |
| TAPE204-10 | 204 | 35 mm | 75x5 mil pads on 10 mil |
| TAPE220-20 | 220 | 35 mm | 75x12 mil pads on 20 mil |
| TAPE244-15 | 244 | 48 mm | 75x8 mil pads on 15 mil |
| TAPE244-20 | 244 | 48 mm | 75x12 mil pads on 20 mil |
| TAPE284-10 | 284 | 35 mm | 75x5 mil pads on 10 mil |
| TAPE284-20 | 284 | 70 mm | 75x12 mil pads on 20 mil |
| TAPE324-15 | 324 | 48 mm | 75x8 mil pads on 15 mil |
| TAPE324-20 | 324 | 70 mm | 75x12 mil pads on 20 mil |
| TAPE364-10 | 364 | 48 mm | 75x5 mil pads on 10 mil |
| TAPE364-20 | 364 | 70 mm | 75x12 mil pads on 20 mil |
| TAPE372-15 | 372 | 70 mm | 75x8 mil pads on 15 mil |
| TAPE404-20 | 404 | 70 mm | 75x12 mil pads on 20 mil |
| TAPE428-15 | 428 | 70 mm | 75x8 mil pads on 15 mil |
| TAPE484-10 | 484 | 48 mm | 75x5 mil pads on 10 mil |
| TAPE484-15 | 484 | 70 mm | 75x8 mil pads on 15 mil |
| TAPE644-10 | 644 | 70 mm | 75x5 mil pads on 10 mil |
| TAPE724-10 | 724 | 70 mm | 75x5 mil pads on 10 mil |
| TAPE804-10 | 804 | 70 mm | 75x5 mil pads on 10 mil |
| MPLCC84 | 84 | Mini plastic LCC (IPC-1-00512) | 75x13 mil pads on .65 mm ctrs |
| MPLCC100 | 100 | | 75x13 mil pads on .65 mm |
| MPLCC132 | 132 | | 75x13 mil pads on .65 mm |
| MPLCC164 | 164 | | 75x13 mil pads on .65 mm |
| MPLCC196 | 196 | | 75x13 mil pads on .65 mm |
| MPLCC244 | 244 | | 75x13 mil pads on .65 mm |
| CFP14 | 14 | Ceramic flat pack | 315x24 mil pads on 1.25 mm ctrs |
| CFP16 | 16 | | 330x24 mil pads on 1.25 mm |
| CFP20 | 20 | | 370x24 mil pads on 1.25 mm |
| CFP24 | 24 | | 400x24 mil pads on 1.25 mm |
| CFP48 | 48 | | 410x10 mil pads on .625 mm |
| CFP56 | 56 | | 410x10 mil pads on .625 mm |

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|---|---|---|---|
| MO-00310 | 10 | Std flat pack IPC-I-00508 | 80x24 mil pads on 50 mil ctrs |
| MO-00410 | 10 | | 80x24 mil pads on 50 mil |
| MO-00314 | 14 | | 80x24 mil pads on 50 mil |
| MO-00414 | 14 | | 80x24 mil pads on 50 mil |
| MO-02116 | 16 | | 80x24 mil pads on 50 mil |
| MO-00416 | 16 | | 80x24 mil pads on 50 mil |
| MO-02220 | 20 | | 80x24 mil pads on 50 mil |
| MO-02124 | 24 | | 80x24 mil pads on 50 mil |
| MO-01924 | 24 | | 80x24 mil pads on 50 mil |
| MO-01928 | 28 | Std flat pack IPC-I-00508 | 80x24 mil pads on 50 mil ctrs |
| MO-02036 | 36 | | 80x24 mil pads on 50 mil |
| MO-02136 | 36 | | 80x24 mil pads on 50 mil |
| MO-02336 | 36 | | 80x24 mil pads on 50 mil |
| MO-02040 | 40 | | 80x24 mil pads on 50 mil |
| MO-01840 | 40 | | 80x24 mil pads on 50 mil |
| MO-02242 | 42 | | 80x24 mil pads on 50 mil |
| MO-02350 | 50 | | 80x24 mil pads on 50 mil |
| PFP14 | 14 | Plastic flat pack | 350x24 mil pads on 50 mil ctrs |
| PFP18 | 18 | | 350x24 mil pads on 50 mil |
| PFP20 | 20 | | 350x24 mil pads on 50 mil |
| PFP28 | 28 | | 350x24 mil pads on 50 mil |
| SOCKET28 | 28 | Surface mt socket | 75x24 mil pads on 50 mil ctrs |
| SOCKET32 | 32 | | 75x24 mil pads on 50 mil |
| SOCKET44 | 44 | | 75x24 mil pads on 50 mil centers |
| SOCKET52 | 52 | | 75x24 mil pads on 50 mil |
| SOCKET68 | 68 | | 75x24 mil pads on 50 mil |
| SO-8 | 8 | Sm outline IC narrow | 80x24 mil pads on 50 mil centers |
| SO-14 | 14 | | 80x24 mil pads on 50 mil |
| SO-16 | 16 | | 80x24 mil pads on 50 mil |
| SOJ-14 | 14 | Sm outline IC J-leaded | 80x24 mil pads on 50 mil centers |
| SOJ-16 | 16 | | 80x24 mil pads on 50 mil |
| SOJ-18 | 18 | | 80x24 mil pads on 50 mil |
| SOJ-20 | 20 | | 80x24 mil pads on 50 mil |
| SOJ-22 | 22 | | 80x24 mil pads on 50 mil |
| SOJ-24 | 24 | | 80x24 mil pads on 50 mil |
| SOJ-26 | 26 | | 80x24 mil pads on 50 mil |
| SOJ-28 | 28 | | 80x24 mil pads on 50 mil |
| JEDEC28 | 28 | Type A Plas leaded chip carrier | 80x24 mil pads on 50 mil centers |
| JEDEC44 | 44 | | 80x24 mil pads on 50 mil |
| JEDEC52 | 52 | | 80x24 mil pads on 50 mil |
| JEDEC68 | 68 | | 80x24 mil pads on 50 mil |

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